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INTELLECTUAL PROPERTY LAW
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAJAT CHAUDHRY, BRIAN KING FLACHS, and DANIEL LAWRENCE STASIAK

Appeal 2009-002612
Application 10/759,936[1]
Technology Center 2100

Before JOSEPH L. DIXON, LANCE LEONARD BARRY, and JAY P. LUCAS, *Administrative Patent Judges.*

LUCAS, *Administrative Patent Judge.*

DECISION ON APPEAL[2]

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[1] Application filed January 16, 2004. The real party in interest is IBM Corp.
[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants appeal from a final rejection of claims 1 to 24 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

We affirm the rejection.

Appellants' invention relates to a method for more accurately approximating power consumption in an integrated circuit by accounting for times when sections of its circuitry are not operational. In the words of Appellants:

> The present invention relates generally to the computer modeling of Very Large-Scale Integration (VLSI) and, more particularly, to more accurately predicting power consumption with computer models.
>
> . . . .
>
> . . . In convention modeling algorithms, the clocks are assumed to be "ON" all of the time or one hundred percent clock activity. Estimations based on one hundred percent clock activity yield an overall maximum of power consumption. The input pins, on the other hand, have associated - switching factors. The switching factors typically range from zero to fifty percent or no switch to one-half of the pins are switching.
>
> By making assumptions that clock activity is at one hundred percent, the power consumption model is in accurate [sic]. When the physical compontents [sic] are actually operating, there are period in which the clock activity may vary. Hence, the power consumption model with one hundred percent clock activity does yield an overall maximum, but does not precisely model the

> activity of a given macro under "real world" conditions.
>
> . . . .
>
> The present invention provides for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs). A Hardware Descriptive Language (HDL) simulator data of the circuit is input. Net capacitance data of the circuit is input. Energy model data is input, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs. Power consumption data is generated from the HDL simulator data, the net capacitance data, and the energy model data.

(Spec. 1, ll. 7 to 10; Spec. 2, ll. 4 to 19; Spec. 3, ll. 1 to 11).

The following illustrates the claims on appeal:

Claim 1:

> 1. A method for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs), comprising:
>
> inputting a Hardware Descriptive Language (HDL) simulator data of the circuit;
>
> inputting net capacitance data of the circuit;
>
> inputting energy model data, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs;
>
> generating power consumption data from the HDL simulator data, the net capacitance data, and the energy model data; and

storing, for subsequent use, an operational model based on the generated power consumption data.

Claim 9:

9. An apparatus for approximating power consumption of a circuit with a plurality of local clock buffers (LCBs), comprising:

means for inputting HDL simulator data of the circuit;

means for inputting net capacitance data of the circuit;

means for inputting energy model data, wherein the energy model data further comprises extrapolating energy data by increasing or decreasing the number of active LCBs;

means for generating power consumption data from the HDL simulator data, the net capacitance data, and the energy model data; and

means for storing, for subsequent use, an operational model based on the generated power consumption data.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Radjassamy	US 2004/086703 A1	Sep. 23, 2004
Lim	US 5,481,209	Jan 02, 1996

REJECTIONS

The Examiner rejects the claims as follows:

R1: Claims 1 to 24 stand rejected under 35 U.S.C. § 103(a) for being obvious over Radjassamy in view of Lim.

(R2): Claims 1 to 24 were rejected under 35 U.S.C. § 112, paragraph 1, for failing to comply with the written description requirement. (Final Rejection mailed 5/18/07 - page 2, ¶ 5.)
Rejection (R2) was withdrawn by the Examiner in the Examiner's Answer.

We will review the rejections in the order argued. We have only considered those arguments that Appellants actually raised in the Brief. Arguments that Appellants could have made but chose not to make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue specifically turns on whether Radjassamy and Lim together teach all of the elements of the claims under appeal, especially the "energy model data … compris[ing] extrapolating energy data by increasing or decreasing the number of active LCBs." (Claims 1, 9).

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants have invented a method of approximating power consumption of an integrated circuit (IC) which, instead of assuming 100% activation of all macros (sections of the IC), calculates the power by an improved formula (Spec. 8, top). Macros are activated by sending an active signal

to the local clock buffer (LCB) of that particular macro. This new formula considers the number of macros on the IC that are actually active, by calculating the ratio of the number of active local clock buffers (LCBAs) to the total number of LCBTs.

2. Appellants' formula is:

(1) Macro Power = (PAR100-PAR0) * (LCBA/LCBT) + PAR0.

> PAR100 corresponds to the power consumption with one hundred percent clock activation, which is essentially the value calculated in conventional modeling methods. PAR0 is the power consumption with no clock activation. LCBA are the number of LCBs that are utilized as a result of the number of active clock signals. LCBT is the total number of LCBs.

(Spec. 8, ll. 9 to 15).

3. The Radjassamy reference estimates the power consumption of an IC (¶ [0004]) in accordance with a formula listed just below. This formula contains a reduction factor F which adjusts the worst case power consumption by taking into consideration the actual clock toggling rate and a flip-flop rate, accounting for their actual usage.

Radjassamy's formula is:

[0047] $P_{EST}=I_{EST}V$

[0048] $$I_{EST} = \sum_{i=1}^{N} I_i P_i F$$

[0049] wherein P_{EST} represents the estimate of power consumption;

[0050] I_{EST} represents the estimate of current;

[0051] V represents voltage;

[0052] P_i represents the number of flip-flops of type i in the sub-block;

[0053] N represents the maximum number of types of flip-flops;

[0054] I_i represents the current of flip-flop type i; and

[0055] F represents the reduction factor for the flip-flops.

(Radjassamy, ¶¶ [0048] to [0055]).

4. The Lim reference teaches that it is known in the prior art that "disabling the local clock buffers for circuits loads not being used in order to reduce power consumption of the integrated circuit." (Lim, col. 6, ll. 1-3).

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

"In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

"It is common sense that familiar items may have obvious uses beyond their primary purposes, and a person of ordinary skill often will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 402 (2007).

ANALYSIS

Arguments with respect to the rejection of claims 1 to 24 under 35 U.S.C. § 103(a) [R1]

The Examiner has rejected the noted claims for being obvious over Radjassamy in view of Lim, indicating that one of ordinary skill in the art would know to substitute for the reduction factor in Radjassamy's equation a reduction factor for the active LCBs, in view of Lim's teachings (Ans., ll. 3 to 7) (*See* FF #2 to #4).

Appellants argue first that "Lim teaches using LCBs to reduce actual power dissipation, not an estimated power dissipation, and certainly not [in the manner claimed]." (Brief 13, top). We have difficulty accepting that a person of ordinary skill in the art would be taught by Lim to disable local clock buffers to reduce power consumption, but would not think to consider that reduction in his estimates of power consumption. Instead we are persuaded that he *would* consider that reduction, and add a reduction factor in his estimate equation, as taught by Radjassamy. (FF#3). The claim only

requires that the formula modifies the energy component in accordance with an increase or decrease in the number of active LCBs. Lim's teaching of disabling LCBs to reduce power we find to be a sufficient teaching.

Appellants then quote Radjassamy, ¶ [0025], and contend that Radjassamy teaches away from Lim's approach (Brief 14, middle). We do not find this argument convincing. In the last sentence of the quoted section, Radjassamy's specification teaches that the purpose of the calculation is "to arrive at an activity factor profile for the component that represents the probabilistic reality of the way its circuitry is designed to operate under normal conditions." (Radjassamy, ¶ [0025]; Brief 14, top). Lim teaches disabling LCBs to reduce power consumption. (FF #4). Neither reference discredits nor discourages the teaching in the other reference, and both are in the field of endeavor of the Appellants. (*See In re Fulton,* 391 F3d 1195, 1201 (Fed. Cir. 2004)). We are thus not persuaded that the rejection is in error, or that the references have been improperly combined.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have not demonstrated that the Examiner erred in rejecting claims 1 to 24.

REJECTION OF CLAIMS 1 TO 24 UNDER 37 C.F.R. § 41.50(B)

We make the following new ground of rejection using our authority under 37 C.F.R. § 41.50(b).

Rejection:

Claims 1 to 24 are rejected under 35 U.S.C. § 112, paragraph 1, for failing to comply with the written description requirement of that statute. During prosecution, Appellants added the limitation "*storing, for subsequent use, an operational model based on the generated power consumption data*" to overcome a rejection under 35 U.S.C. § 101 (Brief 6, top) (Board's emphasis).

The Examiner subsequently rejected Appellants claims with this new limitation under 35 U.S.C. § 112, paragraph 1, indicating that the storing step was not supported by the Specification, failing the written description requirement.

The Examiner chose not to pursue this rejection on Appeal (Ans. 3, top). However, on review of the record before us, we are convinced that the claims are properly rejected under 35 U.S.C. § 112, paragraph 1, and that, should further prosecution ensue, the issue is best addressed now.

Appellants have listed the places in the original Specification that they contend offer support for the noted limitation: Page 10, lines 4 to 8; page 15, lines 18 to 22 (Brief 8, middle). Appellants also point to page 16, lines 18 to 22 as support for this limitation, but this seems to be an error as the referenced section of the Specification is blank (Brief 4, multiple places). Neither the page 10 reference nor the page 15 reference mentions, discusses or alludes to storage of the model. They merely state: "The power modeler 650 can then generate an operational model of the power consumption as the

macro operate [sic] as a Power Data Output 360." Generating the model is not storing it.

PRINCIPLES OF LAW

Under the written description requirement of 35 U.S.C. § 112, the disclosure of the application relied upon must reasonably convey to the artisan that, as of the filing date of the application, the inventor had possession of the later claimed subject matter. *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991). "One shows that one is 'in possession' of *the invention* by describing *the invention,* with all its claimed limitations, not that which makes it obvious." *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) (citing *Vas-Cath*, 935 F.2d at 1563-64).

Although "the meaning of terms, phrases, or diagrams in a disclosure is to be explained or interpreted from the vantage point of one skilled in the art, all the limitations must appear in the specification." *Id.* The specification need not describe the claimed subject matter in exactly the same terms as used in the claims, but it must contain an equivalent description of the claimed subject matter. *Id.*

ANALYSIS

Appellants have argued that storing for future use is well known in the art. We notice, as an aside, that this is a bare assertion by Appellants, and no evidence has been submitted in support of the assertion. However, the standard for written description is not whether the subject matter is well known, but rather whether the specification contains a description of the subject matter. (*See Lockwood v. American Airlines*, cited above.) The specification contains not an iota of recitation describing the storing of the operational model as claimed. Appellants argue that the recitation is

inherent (Brief 10, top). We do not find any inherent disclosure, as there is simply *no* disclosure of storage which could support an inherent limitation as expressed in the claim.

Compliance with the written description requirement is a question of fact which must be resolved on a case-by-case basis. (*See Vas-Cath Inc. v. Mahurkar*, cited above.) We thus find that no support has been demonstrated in the Specification for the claims as presented.

DECISION

We affirm the Examiner's rejection R1 of claims 1 to 24. Moreover, we have entered a new grounds of rejection under 37 C.F.R. § 41.50(b) for claims 1 to 24 as failing to satisfy the written description requirement of 35 U.S.C. § 112, paragraph 1.

With respect to affirmed rejection, 37 C.F.R. § 41.52(a)(1) provides that "Appellant may file a single request for rehearing within two months from the date of the original decision of the Board."

In addition to affirming the Examiner's rejection, this decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b). 37 C.F.R. § 41.50(b) provides that "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that Appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so

> rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

Should Appellants elect to prosecute further before the Examiner pursuant to 37 C.F.R. § 41.50(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the Examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If Appellants elect prosecution before the Examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

37 C.F.R. § 41.50(b)

AFFIRMED

Appeal 2009-002612
Application 10/759,936
peb

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